Thesis Outline

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Abstract

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Introduction

1. LHC.
2. DAQs/YARR.

Single Event Effects

1. Types and their descriptions and relevance to issue.
2. How they effect DAQ (DATA).
3. How they are modeled in HLS and sim.

YARR Rx/Tx Architecture:

1. YARR Tx
   1. Describe how data looks and any important frames that will be sent through
   2. Describe Scrambler + Gearbox, maybe OSERDES
2. YARR Rx
   1. Start with Complete YARR Rx and briefly describe major pieces
   2. Zoom into a lane
      1. Discuss major blocks like ISERDES, Gearbox and Descrambler
      2. Briefly mention recovery system

Original ReSync System

1. Description
   1. The SERDES Bitslip
   2. The Gearbox slip
   3. The Algorithm
2. Performance
   1. The bit drop regression
      1. Recovery time/cycles/slips
      2. Data lost
   2. Random testing
3. Notes for improvement
   1. Smarter searching
   2. Collapse all slips into gearbox
   3. Improve tolerance in algorithm

New ReSync System

1. Additions and Changes
   1. Gearbox slip FSM
   2. Search size parameterization
   3. New Algorithm
2. Performance
   1. Same charts as above
3. Remaining weaknesses

Results Comparison

1. Review the regression comparisons
2. Discuss tolerance implications
3. Review random testing comparisons

Future Works

Acknowledgements

References